

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number 10001477

Filing Date 2001-11-01

First Named Inventor Steve Roe

Art Unit 2123

Examiner Name Jason Scott Proctor

Attorney Docket Number CD01203M

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code*	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7042301	B1	2006-05-09	Sufardja, Sehat	Entire Document
	2	5594398	B1	1997-01-14	O'Shaughnessy et al.	Entire Document
	3	5963105	B1	1999-10-05	Nguyen	Entire Document
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Examiner Name	Jason Scott Proctor	
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10	7250825	B1	2007-07-31	Wilson et al.	Entire Document
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Attorney Docket Number	CD01203M	

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	1	Application Number 11/850,260 (CD2007006): "Circuit and Method for Improving the Accuracy of a Crystal-less Oscillator Having Dual-Frequency Modes;" Wright et al.; 33 pages	<input type="checkbox"/>
	2	USPTO Non-Final Rejection for Application Number 11/850,260 (CD2007006) dated 03/06/2009; 7 pages	<input type="checkbox"/>
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	4	USPTO Advisory Action for Application Number 11/644,100 (CD05204) dated 02/09/2009; 3 pages	<input type="checkbox"/>
	5	USPTO Final Rejection for Application Number 11/644,100 (CD05204) dated 11/18/2008; 12 pages	<input type="checkbox"/>

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Attorney Docket Number	CD01203M

6	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 04/14/2006; 10 pages	<input type="checkbox"/>
7	USPTO Notice of Allowance for Application Number 11/415,588 (CD05028) dated 03/11/2008; 6 pages	<input type="checkbox"/>
8	USPTO Advisory Action for Application Number 11/415,588 (CD05028) dated 01/14/2008; 3 pages	<input type="checkbox"/>
9	USPTO Final Rejection for Application Number 11/415,588 (CD05028) dated 10/19/2007; 8 pages	<input type="checkbox"/>
10	USPTO Non-Final Rejection for Application Number 11/415,588 (CD05028) dated 06/13/2007; 8 pages	<input type="checkbox"/>
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12	USPTO Non-Final Rejection for Application Number 12/218,404 (CD05028C1) dated 09/30/2008; 6 pages	<input type="checkbox"/>
13	Application Number 11/644,100 (CD05204): "Differential-to-single ended signal converter circuit and method." Stiff, 33 pages	<input type="checkbox"/>
14	Application Number 11/415,588 (CD05028): "Voltage Controlled Oscillator Delay Cell and Method." Sivadasan; 24 pages	<input type="checkbox"/>
15	Application Number 12/218,404 (CD05028C1): "Voltage Controlled Oscillator Delay Cell and Method." Sivadasan, 23 pages	<input type="checkbox"/>
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Attorney Docket Number	CD01203M

17	USPTO Non-Final Rejection for Application Number 11/132,894 (CD04064) dated 12/19/2006; 12 pages	<input type="checkbox"/>
18	Application Number 11/132,894 (CD04064): "Open Loop Bandwidth Test Architecture and Method for Phase Locked Loop (PLL)," Still; 36 pages	<input type="checkbox"/>
19	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 05/04/2008; 18 pages	<input type="checkbox"/>
20	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 11/25/2008; 15 pages	<input type="checkbox"/>
21	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 04/11/2008; 11 pages	<input type="checkbox"/>
22	USPTO Advisory Action for Application Number 11/322,044 (CD05198) dated 11/30/2007; 2 pages	<input type="checkbox"/>
23	USPTO Final Rejection for Application Number 11/322,044 (CD05198) dated 09/21/2007; 14 pages	<input type="checkbox"/>
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28	USPTO Non-Final Rejection for Application Number 10/305,589 (CD02181) dated 10/07/2003; 6 pages	<input type="checkbox"/>
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30	Application Number 09/849,164 (CD01035): "Reduced Static Phase Error CMOS PLL Charge Pump," Sliff; 30 pages	<input type="checkbox"/>
31	Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; 10 pages	<input type="checkbox"/>
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34	USPTO Non-Final Rejection for Application Number 10/327,217 (CD02174) dated 04/30/2004; 5 pages	<input type="checkbox"/>
35	USPTO Miscellaneous Action for Application Number 10/327,217 (CD02174) dated 02/10/2004; 1 page	<input type="checkbox"/>
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37	USPTO Notice of Allowance for Application Number 10/871,582 (CD03036) dated 03/30/2006; 6 pages	<input type="checkbox"/>
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39	USPTO Non-Final Rejection for Application Number 10/871,582 (CD03036) dated 09/07/2005; 7 pages	<input type="checkbox"/>
40	Application Number 10/871,582 (CD03036): "LVDS Input Circuit with Extended Common Mode Range," Reinschmidt et al.; 25 pages	<input type="checkbox"/>
41	USPTO Notice of Allowance for Application Number 09/404,891 (CD99054) dated 03/04/2005; 6 pages	<input type="checkbox"/>
42	USPTO Final Rejection for Application Number 09/404,891 (CD99054) dated 12/06/2004; 7 pages	<input type="checkbox"/>
43	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 06/25/2004; 6 pages	<input type="checkbox"/>
44	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 01/05/2004; 5 pages	<input type="checkbox"/>
45	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 07/10/2003; 5 pages	<input type="checkbox"/>
46	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 03/05/2003; 5 pages	<input type="checkbox"/>
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48	Application Number 09/404,891 (CD99054): "Method, Architecture and Circuitry for Controlling Pulse Width in a Phase and/or Frequency Detector," Scott et al.; 17 pages	<input type="checkbox"/>
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50

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	2	6660306	B1	2003-05-06	Duffy et al.	Entire Document
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1	20050280453	A1	2005-12-22	Hsieh	Entire Document
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	3	USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 08/26/2003; 9 pages	<input type="checkbox"/>
	4	USPTO Final Rejection for Application Number 09/943,149 (CD01085) dated 05/07/2003; 10 pages	<input type="checkbox"/>
	5	USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 11/20/2002; 7 pages	<input type="checkbox"/>

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6	Application Number 09/043,149 (CD01085): "Method for Phase Locking in a Phase Lock Loop," Moyal et al.; 21 pages	<input type="checkbox"/>
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12	Application Number 09/471,914 (CD99064): "Reference-Free Clock Generator and Data Recovery PLL," Dalmia et al.; 32 pages	<input type="checkbox"/>
13	Application Number 09/471,576 (CD99062): "Reference-Free Clock Generation and Data Recovery PLL," Dalmia; 30 pages	<input type="checkbox"/>
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Attorney Docket Number	CD01203M	

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Application Number		10001477
Filing Date		2001-11-01
First Named Inventor	Steve Roe	
Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Attorney Docket Number	CD01203M	

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(Not for submission under 37 CFR 1.99)

Application Number		10001477
Filing Date		2001-11-01
First Named Inventor	Steve Roe	
Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Application Number	10001477
Filing Date	2001-11-01
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Art Unit	2123
Examiner Name	Jason Scott Proctor
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number		10001477
Filing Date		2001-11-01
First Named Inventor	Steve Roe	
Art Unit	2123	
Examiner Name	Jason Sooti Proctor	
Attorney Docket Number	CD01203M	

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First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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U.S. PATENTS

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(Not for submission under 37 CFR 1.99)

Application Number	10001477
Filing Date	2001-11-01
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Art Unit	2123
Examiner Name	Jason Sooti Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123	
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Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123	
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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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(Not for submission under 37 CFR 1.99)

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Filing Date	2001-11-01
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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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(Not for submission under 37 CFR 1.99)

Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Stevn Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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	First Named Inventor	Steve Roe	
	Art Unit	2123	
	Examiner Name	Jason Scott Proctor	
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Filing Date	2001-11-01
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Art Unit	2123
Examiner Name	Jason Scott Proctor
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Art Unit	2123	
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Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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	1	Kory Hopkins, "Definition," 01/16/1997; < http://www.cs.sfu.ca/cs/people/GradStudent.html >, 1 page	<input type="checkbox"/>
	2	Ebeling et al., "Validating VLSI Circuit Layout by Wirelist Comparison," Sept. 1993; in proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-93); 2 pages	<input type="checkbox"/>
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(Not for submission under 37 CFR 1.99)

Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

8	International Search Report from the International Search Authority for International Application Number PCT/US08/60680 (CD2007130PCT) dated 08/15/2008; 4 pages	<input type="checkbox"/>
9	USPTO Notice of Allowance for Application Number 09/475,879 (CD99047) dated 10/22/2004; 7 pages	<input type="checkbox"/>
10	USPTO Advisory Action for Application Number 09/475,879 (CD99047) dated 03/04/2002; 3 pages	<input type="checkbox"/>
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12	USPTO Final Rejection for Application Number 09/475,879 (CD99047) dated 10/11/2001; 10 pages	<input type="checkbox"/>
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	10001477
Filing Date	2001-11-01
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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10001477
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Application Number	10001477
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First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

4	USPTO Notice of Allowance for Application Number 11/273,708 (CD05141) dated 08/09/2007, 4 pages	<input type="checkbox"/>
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Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

15	USPTO Non-Final Rejection for Application Number 11/698,660 (CD05176) dated 12/02/2008; 12 pages	<input type="checkbox"/>
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Art Unit	2123
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Attorney Docket Number	CD01203M

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U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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**INFORMATION DISCLOSURE
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Filing Date		2001-11-01
First Named Inventor	Steve Roe	
Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	10001477
Filing Date	2001-11-01
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Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD91203M	

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U.S. PATENTS

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Filing Date		2001-11-01
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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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Art Unit	2123	
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Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

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